



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Pechanek (et al.)

Serial No.:

10/774,815

Filed:

February 9, 2004

For:

MANIFOLD ARRAY PROCESSOR

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date set forth below:

Signed: Mauera

Name: Marianna Tortorelli

Date: March 5, 2004

Durham, North Carolina March 5, 2004

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is being filed before the receipt of a first Official Action. Pursuant to 37 C.F.R. 1.56, 1.97 and 1.98, applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following items cited in the attached European Search Report and listed on the accompanying Form PTO/SB/08A. The undersigned certifies that each item of information contained in this statement was first cited in any communication from a foreign patent office in a counterpart foreign application dated February 18, 2004, which is not more than three months prior to the filing of this statement.

The Commissioner is authorized to charge any fees or credit any overpayments to Law Offices of Peter H. Priest Deposit Account No. 50-1058.

ITEMS

Publication Date Patentee/Applicant

1. EP 0569763 A 11//18/1993 International Business Machines Corporation

Other Publications

2. PECHANEK ET AL., M.F.A.S.T.: A Single Chip Highly Parallel Image Processing Architecture, Proceedings of the International Conference on Image Processing (ICIP), 10/23/1995, Page(s) 69-72, Volume 3, Publisher: IEEE Comp. Soc. Press

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made nor shall it be construed as an admission that the information cited is considered to be material to patentability, nor shall it be construed that no other material information exists.

Respectfully submitted,

Reg. No. 52,547

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RAI END

PTO/SB/08a (08-03)
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ABO				Complete if Known			
Sub	bstitute for form 1449A/PTO			Application Number	10/774,815		
I N	NFORMATION DISCL	OS!	IDE	Filing Date	02/09/2004		
				First Named Inventor	Pechanek et al.		
3	STATEMENT BY APP	LIC	ANI	Art Unit			
	(Use as many sheets as neces	ssary)		Examiner Name			
Sheet	1	of	2	Attorney Docket Number	800.0133		

U.S. PATENT DOCUMENTS									
Examiner	Cite	Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where				
Initials*	No.1	Number - Kind Code ^{2 (# known)}	MM-DD-YYYY	Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear				
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	FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No.1	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶			
		EP0569763	11/18/1993	International Business Machines Corp.					

Examiner	•		Date		
Signature			Considered		
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Substitute for form 1449B/PTO				Complete if Known		
0000				Application Number	10/774,815	
INF	ORMATION DISC	u osi	IRF	Filing Date	02/09/2004	
				First Named Inventor	Pechanek et al.	
317	STATEMENT BY APPLICANT			Art Unit		
(Use as many sheets as necessary)				Examiner Name		
Sheet 2 of 2		Attorney Docket Number	800.0133			

NON PATENT LITERATURE DOCUMENTS							
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²				
		PECHANEK ET AL., M.F.A.S.T.: A Single Chip Highly Parallel Image Processing Architecture, Proceedings of the International Conference on Image Processing (ICIP), 10/23/1995, Page(s) 69-72, Volume 3, Publisher: IEEE Comp. Soc. Press					
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